32.7 A 2GHz 0.25µm SiGe BiCMOS Oscillator with Flip-Chip Mounted BAW Resonator

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The design and integration of a BAW/BiCMOS IC co-integrated RF oscillator for 2G to 4G mobile communications applications is presented. The Bulk Acoustic Wave (BAW) resonator is realized using Solidly Mounted Resonator (SMR) technology and is then assembled by flip-chip bumping on top of a 0.25µm SiGe:Carbon BiCMOS die. The 2GHz oscillator achieves a -124dBc/Hz phase noise at 100kHz carrier offset, while the oscillator core consumes 4.8mA with 2.5V supply. Although designed as a proof of BAW/IC co-integration, the oscillator is compliant with GSM requirements. The use of a commercial SiGe BiCMOS process enables the fast introduction of such a solution into mobile communication transceivers. In recent years, several methodologies for BAW/IC co-integration have been developed to obtain high performance RF oscillators / front-ends in the frequency range of 2 to 15GHz [1,2,3,4]. Some of them, focusing on SoC integration, are using Above-IC (A-IC) post-processing in order to obtain either FBARs [1,2] or high-quality inductors [4]. Drawbacks of that approach are high technology cost and large die area, as the A-IC device may not be placed directly on top of the RF core. An alternative is SiP integration. Work on oscillators and VCOs reported so far has relied on chip-to-chip wire-bonding [3], resulting in a large module area and floor-planning and packaging constraints.

A SiP approach is presented where the SMR is directly flip-chipped on the top of the RF active core, resulting in a very compact assembly (170×250×560µm³) and enhanced phase noise performance. The BAW resonator is characterized by a series (f_s) and a parallel (f_p) resonance frequency. It is equivalent to a low impedance at f_s and to a high impedance at f_p. Out of the f_s-f_p band, it is seen as a capacitor C_o, whereas inside this band it behaves as an inductor. The modified Butterworth-Van Dyke model has been used to represent the resonator's electrical behavior. Only the series resistor R_s, representing the ohmic losses in the electrodes, is associated with noise. Noise phenomena in the piezoelectric layers are still poorly modeled. When assimilated to frequency instability, noise is generated by environmental perturbations like temperature, acceleration or electromagnetic fields and by variations in the piezoelectric materials like impurity migration or random vibrations.

The oscillator implemented here uses the well-known Colpitts technique (see Fig. 32.7.1). A negative resistance is created by a bipolar device in a common collector configuration. Its expression is given by $-\frac{g_m}{C_1 C_2 \omega^2}$. The inductive behavior of the BAW resonator in the f_s-f_p frequency band is exploited to generate the oscillations by resonating with the load capacitance C_L. The oscillation frequency can be expressed by:

$f_{osc} = f_s\left(1+\frac{C_m}{2(C_o+C_L)}\right)$, where $C_L = \frac{(C_1+C_\pi)C_2}{C_1+C_\pi+C_2}$ (C_π from the bipolar transistor)

Concerning the oscillator's phase noise optimization, classical criteria apply also for this design. Phase noise minimization is obtained by a maximization of the signal amplitude, thus decreasing the C_2 capacitor. However, it is convenient to limit the signal amplitude on the BAW terminals in order not to increase BAW 1/f noise near the carrier. Indeed, higher signal amplitude increases the risk of instabilities. Oscillator design considerations imply the lowest possible sensitivity to process variations in order to implement a robust oscillator generating an accurate oscillation frequency. Finally, a 50Ω on-chip buffer has been implemented for test purposes.

This design employs a 1.77pF-C_o SMR with a 2.124GHz resonant frequency, a Q-factor of about 600 and a coupling coefficient k_t^2 of 6.5%. The resultant 2.145GHz oscillator consumes 4.8mA with 2.5V supply. It is interesting to note that a decrease in the supply voltage will not considerably impact the phase noise performance as depicted in the table shown in Figure 32.7.2. A phase noise of -124dBc/Hz has been measured at a 100kHz offset from the carrier for a standard 2.5V supply voltage. At larger offsets, the noise floor reaches -160dBc/Hz and is probably limited by the output buffer performance. Nevertheless, one can observe that noise in the vicinity of the oscillation frequency is underestimated as no specific BAW noise model is used. The accuracy of the oscillation frequency, mainly dependent on the BAW resonance frequency, has been measured over several circuits with oscillation frequency dispersion lower than 1.3MHz (600ppm). Excellent supply voltage rejection has been obtained as shown in Figure 32.7.3 with an accuracy of 65ppm/V. Figure 32.7.7 presents a micrograph of the circuit; one can observe the 120×200µm² BAW resonator flip-chipped on top of the active core of the oscillator. The assembly of the two chips is performed using gold bumps, as depicted in Figure 32.7.4. The passivation openings on the SiGe die are placed in close proximity to the active core of the oscillator. This assembly method is fully compatible with production SiP integration. As observed from the measured results, no significant spurious behavior is induced by the presence of the resonator on the top of the very sensitive active core of the oscillator.

To conclude, experimental results were presented for a 2.145GHz oscillator integrating SMR BAW resonators and BiCMOS technologies via chip-to-chip flip-chip assembly. The circuit achieves stringent GSM phase noise and stability performance requirements, a reduced IC foot-print and very competitive power consumption, as summarized in Figure 32.7.5. The ITRS FOM for oscillators places the circuit among a new category of high-performance MEMS oscillators (see Fig. 32.7.6). Measurements show good agreement with post-layout simulations. Switchable capacitances or varicaps could be used to properly compensate oscillation frequency drifts providing interesting possibilities for RF frequency synthesis. This experimental test-chip opens new opportunities towards SiP integration, by using BAW resonators traditionally dedicated to RF filtering for close passive/active co-integration in frequency synthesis.

Acknowledgements:
The authors acknowledge the contributions of the following people: P. Ancey, G. Caruyer, F. Dumont, F. Badets, A. Spataro, C. Arnaud from STMicroelectronics and M. Aïd and G. Parat from CEA/LETI and Y. Gamberini.

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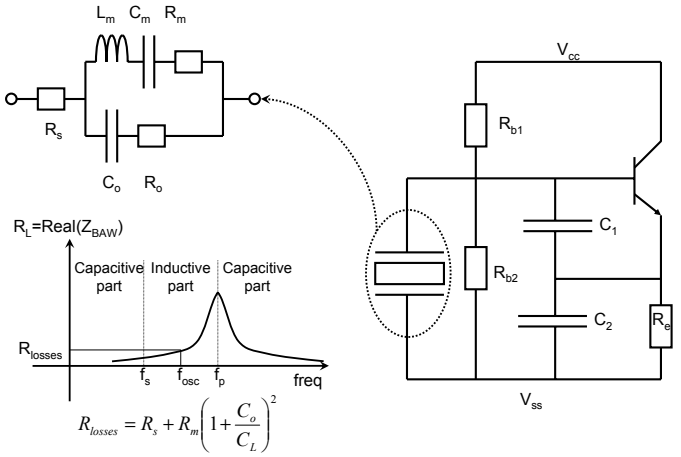
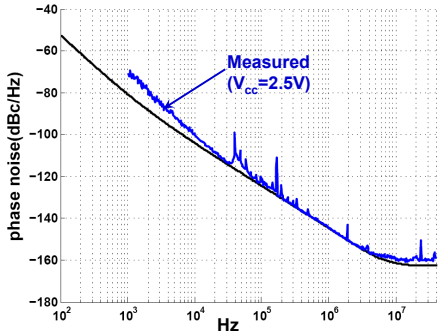


Figure 32.7.1: Oscillator schematic with BAW electrical model.



V_{cc} (V)	2	2.3	2.5	2.7
Current consumption (mA)	3.4	4.2	4.8	5.4
Phase noise @100kHz (dBc/Hz)	-118.4	-122.8	-124	-124.3
Oscillation frequency (GHz)	2.14942	2.149482	2.149484	2.149476
FOM (dB)	-196.7	-199.6	-199.85	-199.3

Figure 32.7.2: Phase noise measurement results.

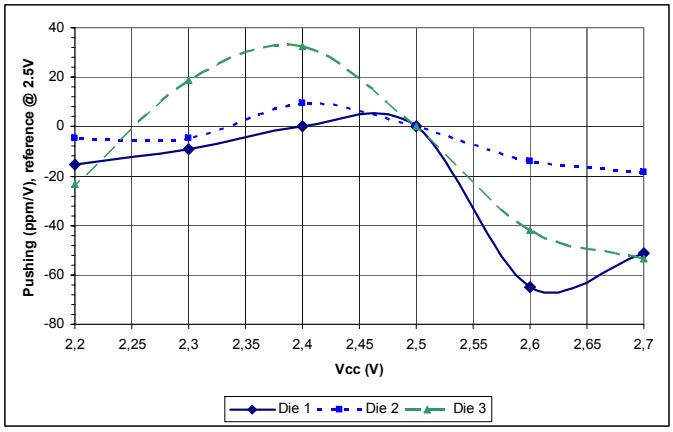


Figure 32.7.3: Measured oscillator pushing.

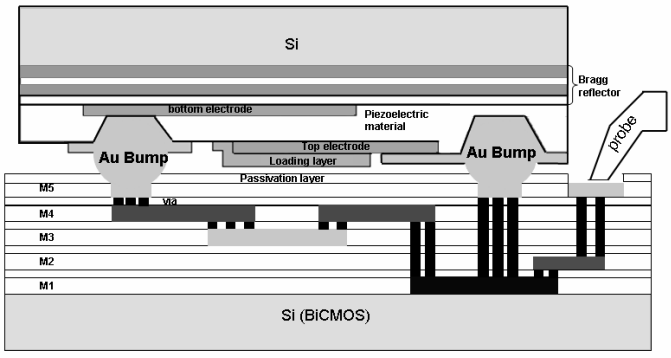


Figure 32.7.4: Assembly cross-section.

Parameter	Value
Oscillation frequency	2.145GHz
Core power consumption	4.8mA × 2.5V
Phase Noise @ 100kHz	-124dBc/Hz
Phase Noise Floor	-160dBc/Hz
Pushing	65ppm/V
Oscillation frequency precision	600ppm
FOM [4]	-199.8dB
Si Core foot-print	0.043mm²

Figure 32.7.5: BAW oscillator measured performance.

Ref.	Process Architecture	fosc (GHz)	Vcc (V)	Icc (mA)	Phase noise (dBc/Hz)	Fm (kHz)	Phase noise floor (dBc/Hz)	FOM [4] (dB)	Size area (mm²)
This work	BiCMOS 0.25µm MEMS oscillator	2.145	2.5	4.8	-124	100	-160	**-199.8**	**0.043**
[2]	BiCMOS 0.35µm MEMS oscillator	5.4	2.7	1.7	-117.7	100	n.a.	**-205.7**	**0.539**
[3]	CMOS 0.18µm MEMS oscillator	1.9	1	0.3	-120	100	-150	**-210.8**	**0.514**
[5]	BiCMOS 0.6µm MEMS VCO	1.215	3.3	3	-110.9	100	n.a.	**-182.6**	n.a
[4]	CMOS 90nm A-IC LC VCO	6.3	1.2	4.9	-118	1000	n.a.	**-195.1**	**0.4**
[6]	BiCMOS A-IC LC VCO	1.9	3.3	5.5	-106	100	~-130	**-179**	**0.77**
[7]	CMOS SOI 0.13µm LC VCO	4.4	1	2	-114.6	1000	-126	**-187.1**	**0.3**
[8]	BiCMOS 0.25µm LC VCO	3.8	1.9	8	-119.46	400	-143	**-187.2**	**0.354**
[9]	CMOS 0.25µm LC VCO	2.4	1	4.6	-136	3000	~-150	**-187.4**	**0.874**
[10]	CMOS 0.35µm LC VCO	2.2	1.4	9	-139	3000	~-150	**-185.3**	**0.935**

Figure 32.7.6: Summary of high performance oscillators and VCOs.

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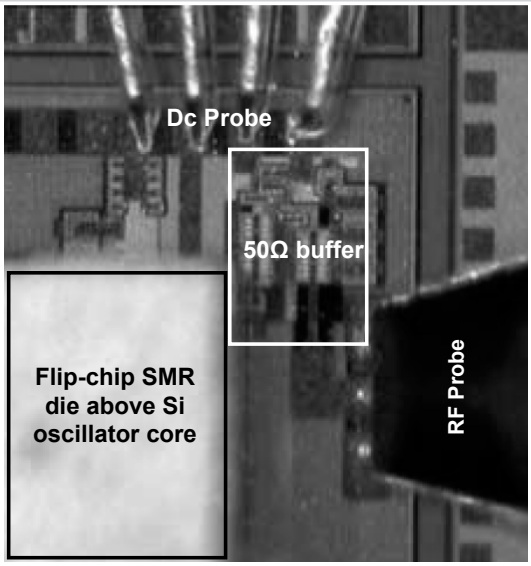

Figure 32.7.7: BAW oscillator micrograph.

